Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **D1**
2. **NC**
3. **D3**
4. **S3**
5. **S4**
6. **D4**
7. **NC**
8. **D2**
9. **S2**
10. **IN2**
11. **V+**
12. **VL**
13. **GND**
14. **V-**
15. **IN1**
16. **S1**

**.070”**

**1 16 15**

**3**

**4**

**5**

**6**

**7 8 9 10**

**14**

**13**

**12**

**11**

**AG58Z-1Z**

**MASK**

**REF**

**A**

**.102”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004 x .004”**

**Backside Potential:**

**Mask Ref: AG58Z-1Z**

**APPROVED BY: DK DIE SIZE .070” X .102” DATE: 3/10/22**

**MFG: MAXIM THICKNESS .015” P/N: DG403C/D**

**DG 10.1.2**

#### Rev B, 7/1